ABSTRACT

A random access memory includes a first memory bank, a second memory bank, an error checking circuit operatively connected to receive data read from the first memory bank, and a multiplexer operatively connected to input data read from both the first memory bank and the second memory bank, wherein input selection of the multiplexer is controlled by an output of the error checking circuit. A method for reducing errors in a memory system includes writing data into first and second memory banks of the memory system in parallel, reading data from a desired location of the first memory bank, checking the data read from the first memory bank for errors, if no errors are present, outputting the data read from the first memory bank to a bus, and if the data read from the first memory bank contains errors, outputting data read from a parallel location in the second memory bank to the bus. A method for reducing errors in a memory system comprises writing data into first and second memory banks of the memory system in parallel, reading data from a desired location of the first memory bank, checking the data read from the first memory bank for errors, if no errors are present, outputting the data read from the first memory bank to a bus, and if the data read from the first memory bank contains errors, outputting data read from a parallel location in the second memory bank to the bus.

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